



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: 40296-0048

Applicant: Seon Yong CHA

Confirmation No.: 1788

Appl. No.: 10/734,294

Examiner: Thomas L. Dickey

Filing Date: December 15, 2003

Art Unit: 2826

Title: MAGNETORESISTIVE RANDOM ACCESS MEMORY, AND  
MANUFACTURING METHOD THEREOF

**INFORMATION DISCLOSURE STATEMENT  
UNDER 37 CFR §1.56 and 37 CFR §1.97**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Submitted herewith on Form PTO/SB/08A is a listing of documents known to applicant in order to comply with applicant's duty of disclosure pursuant to 37 C.F.R. §1.56 and §1.97. A copy of the listed documents are being submitted to comply with the provisions of 37 C.F.R. §1.97-1.99.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or is considered to be material to patentability as defined in 37 C.F.R. §1.56(b). Applicant does not waive any rights to take any action that would be appropriate to antedate or otherwise remove as a competent reference any document that is determined to be a *prima facie* prior art reference against the claims of the present application.

**RELEVANCE STATEMENT**

The foregoing documents came to the Applicant's attention during a search of the corresponding German patent application. A copy of the Notice of Rejection from the German Patent Office is attached.



U.S. Applic. No. 10/734,294

TIMING/FEEs

Based on 37 CFR 1.97(i), Applicants request that the references cited on the attached SB/08A form be placed in the file and Applicant acknowledges that the references cited will not be considered by the Examiner.

Date: 2/2/06

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Respectfully submitted,

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Substitute for form 1449A/PTO

## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

*(use as many sheets as necessary)*

Sheet	1	of	2
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**Complete if Known**

Application Number	10/734,294
Filing Date	December 15, 2003
First Named Inventor	Seon Yong CHA
Group Art Unit	2826
Examiner Name	Thomas L. Dickey
Attorney Docket Number	40296-0048

## U.S. PATENT DOCUMENTS

[illegible]

## FOREIGN PATENT DOCUMENTS

[illegible]

Examiner  
Signature

Date  
Considered

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04.

<sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449A/PTO		<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)		Application Number	10/734,294
		Filing Date	December 15, 2003
		First Named Inventor	Seon Yong CHA
		Group Art Unit	2826
		Examiner Name	Thomas L. Dickey
Sheet 2 of 2	Attorney Docket Number	40296-0048	

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	C09	XIANGDON CHEN et al., "Improved Hot-Carrier and Short-Channel Performance in Vertical nMOSFETs With Graded Channel Doping", IEEE Transactions on Electron Devices, 2002, p. 1962-1967, Vol. 49, No. 11	
	C10	W.J. GALLAGHER et al., "Microstructured magnetic tunnel junctions (invited)", J. Appl. Phys., 1997, pp. 3741-3746, Vol. 81, No. 8	
	C11	GITAE JEONG et al., "Magnetoresistance RAM with Self Reference Sensing. In: IEEE International Solid-State Circuits Conference, 9-13 Feb. 2003, S.1-8; "dual gate polysilicon", "Serially connected MTJ", A 0.24um 2.0V 1T1MTJ 16kb NV	
	C12	ABHINAV KRANTI et al., "Design Guidelines of Vertical Surrounding Gate (VSG) MOSFETs for Future ULSI Circuit Applications", IEEE, 2001, pp. 161-165	
	C13	K. McSTAY et al., "Vertical Pass Transistor Design for Sub-100nm DRAM Technologies", IEEE, Symposium On VLSI Technology Digests of Technical Papers, 2002, pp. 180-181	
	C14	Q. OUYANG et al., "Performance Enhancement in Vertical Sub-100NM NMOSFETS with Graded Doped Channels", IEEE, 2002, Fourth IEEE International Caracas Conference on Devices, Circuits and Systems, Aruba, April 17-19, 2002, pp. DO16-1, DO16-6	
	C15	WILLIAM REOHR et al., "Memories of Tomorrow", IEEE Circuits and Devices Magazine, September 2002, pp. 17-27	
	C16	G. SHRIVASTAV et al., "Performance Optimization of 60nm Channel Length Vertical MOSFETs Using Channel Engineering", IEEE, 2000, pp. 475-478	

Examiner Signature	Date Considered
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